Claims:

1. A method for performing a mask design layout resolution enhancement, comprising:

determining a first level of correction for the mask design layout for a predetermined parametric yield with a minimum total correction cost; and

correcting the mask design layout at said first level of correction based on a correction algorithm if said first level of correction is determined to be required.

2. The method as defined in claim 1 wherein said determining said first level of correction includes obtaining a probability density function of circuit performance of the mask design layout.

3. The method as defined in claim 2 wherein said probability density function is obtained using a statistical static timing analysis (SSTA).

4. The method as defined in claim 3 wherein said probability density function is compared with said predetermined parametric yield with said minimum total correction cost to determine said first level of correction.

5. The method as defined in claim 4 wherein the mask design layout is not corrected if it is determined that said first level of correction is not required.

6. The method as defined in claim 1 further including determining a second level of correction for the mask design layout for said predetermined parametric yield after correcting the mask at said first determined level of correction.

7. The method as defined in claim 6 further including, correcting the mask design layout at said second level of correction based on said correction algorithm if said second level of correction is determined to be required.

8. The method as defined in claim 7 wherein the mask design layout is not corrected if it is determined that said second level of correction is not required.

9. The method as defined in claim 1 wherein said correction algorithm is based on an assumption that a standard deviation of gate delays of the mask design layout are additive.

10. The method as defined in claim 9 wherein said correction algorithm is based on an assumption that

$$\mu_{1+2} + k\sigma_{1+2} = \mu_1 + k\sigma_1 + \mu_2 + k\sigma_2$$

where $\mu+k\sigma$ is where μ is the mean, σ is the standard deviation of the performance distribution of gates, and $\mu+k\sigma$ denotes a certain level of parametric yield.

11. The method as defined in claim 10 wherein said correction algorithm is a mathematical programming problem expressed as,

$$\textit{Minimize} \sum_{i,j} x_{ij}$$
$$\sum_j x_{ij} = 1$$
$$\sum_j x_{ij}\, d_{ij} + wd_i < wd_k \quad \forall\, k \in \textit{fanout}(i)$$
$$wd_k = U \quad \forall \; k \in PO$$
$$x_{ij} \in \{0,1\}$$

where,

$d_{ij} = \mu + k\sigma$ number for gate i corresponding to level of correction j,

c_{ij} = cost of correction number for gate i corresponding to level of correction j,

$x_{ij} = 1$ if gate i is corrected to level j,

wd_i = worst case $\mu + k\sigma$ delay at input of gate i, calculated using STA,

$U = \mu + k\sigma$ delay upper bound at the primary outputs (POs),

12. The method as defined in claim 10 wherein said correction algorithm is obtained by mapping to an area, a nominal delay, a cycle time and a die area of a gate sizing problem.

13. The method as defined in claim 12 wherein said correction algorithm is a obtained by mapping an area, a nominal delay, a cycle time and a die area of said gate sizing problem with a cost of correction, delay $\mu+k\sigma$, selling point delay and total cost of resolution enhancement technique (RET), respectively.

14. The method as defined in claim 13 wherein a yield library having said predetermined parametric yield is constructed to have a form of a timing library.

15. The method as defined in claim 1 wherein said predetermined parametric yield is obtained from a yield library, wherein said yield library captures delay mean and variance for each level of correction for each library master, and a relative cost of resolution enhancement technique (RET) at each level of correction for said each master.

16. A method for minimizing a cost of correction of a mask design layout, comprising:

obtaining a first probability density function of a signal arrival time at an output of the circuit on the mask design layout;

determining whether said first probability density function satisfies a predetermined parametric yield with a minimum total correction cost;

correcting the mask design layout at a first level of correction based a correction algorithm if said first probability density function does not satisfy said predetermined parametric yield with a minimum total correction cost.

17. The method as defined in claim 16 wherein said first probability density function is obtained using a statistical static timing analysis (SSTA).

18. The method as defined in claim 16 wherein the mask design layout is not corrected if said first probability density function satisfies said predetermined parametric yield with said minimum total correction cost

19. The method as defined in claim 16 further including:

determining a second probability density function of an arrival time at output of the circuit on the mask design layout after correcting the mask design layout at said first determined level of correction; and

determining whether said second probability density function satisfies said predetermined parametric yield with a minimum total correction cost; and

correcting the mask design layout at a second first level of correction based on said correction algorithm if said second probability density function satisfies said predetermined parametric yield with a minimum total correction cost, and not correcting the mask design layout if said second probability density function satisfies said predetermined parametric yield with a minimum total correction cost.

20. The method as defined in claim 16 wherein said correction algorithm is based on an assumption that a standard deviation of gate delays of the mask design layout are additive.

21. The method as defined in claim 20 wherein said correction algorithm is based on an assumption that

$$\mu_{1+2} + k\sigma_{1+2} = \mu_1 + k\sigma_1 + \mu_2 + k\sigma_2$$

where $\mu+k\sigma$ is where μ is the mean, σ is the standard deviation of the performance distribution of gates, and $\mu+k\sigma$ denotes a level of parametric yield.

22. The method as defined in claim 21 wherein said correction algorithm is a mathematical programming problem expressed as,

$$\textit{Minimize} \sum_{i,j} x_{ij}$$

$$\sum_j x_{ij} = 1$$

$$\sum_j x_{ij}\, d_{ij} + wd_i < wd_k \quad \forall\, k \in \textit{fanout}(i)$$

$$wd_k = U \quad \forall \quad k \in PO$$

$$x_{ij} \in \{0,1\}$$

where,

$d_{ij} = \mu + k\sigma$ number for gate i corresponding to level of correction j,

c_{ij} = cost of correction number for gate i corresponding to level of correction j,

$x_{ij} = 1$ if gate i is corrected to level j,

wd_i = worst case $\mu + k\sigma$ delay at input of gate i, calculated using STA, and

$U = \mu + k\sigma$ delay upper bound at the primary outputs (POs).

23. The method as defined in claim 21 wherein said correction algorithm is obtained by mapping to an area, a nominal delay, a cycle time and a die area of a gate sizing problem.

24. The method as defined in claim 23 wherein said correction algorithm is a obtained by mapping an area, nominal delay, cycle time and die area of the gate sizing problem with a cost of correction, delay $\mu+k\sigma$, selling point delay and total cost of resolution enhancement technique (RET), respectively.

25. The method as defined in claim 24 wherein an yield library having said predetermined parametric yield is constructed to have a form of a timing library.

26. The method as defined in claim 16 wherein said predetermined parametric yield is obtained from a yield library which captures performance mean and variance for each level of correction for each library master, and a relative cost of resolution enhancement technique (RET) at each level of correction for said each master.

27. A method for performing a mask design layout resolution enhancement comprising:

determining a tolerable performance variation for each of a plurality of features in the mask design layout;

determining a critical dimension (CD) variation tolerance corresponding to said tolerable performance variation for said each of said plurality of features;

determining an edge placement error (EPE) tolerance corresponding to said CD variation tolerance for said each of said plurality of features; and

correcting each of said plurality of features so that at least one edge on said each of said plurality of features prints within tolerance based on said EPE tolerance.

28. The method as defined in claim 27, wherein said tolerable performance variation for said each of said plurality of features is determined using a performance budgeting algorithm.

29. The method as defined in claim 27, wherein said critical dimension (CD) variation tolerance is determined from said tolerable performance variation using dependences of performance on critical dimension (CD).

30. The method as defined in claim 27, wherein said at least one edge on said each of said plurality of features is corrected by implementing a resolution enhancement technique (RET) based on said on said EPE tolerance.

31. A machine readable medium for storing a program in a system for performing a mask design layout resolution enhancement in which a level of correction for the mask design layout for a predetermined parametric yield with a minimum total correction cost is determined, and the mask design layout is corrected at the determined level of correction based on the program on the medium if the level of correction is determined to be required, said program comprising:

a mathematical program expressed as,

$$Minimize \sum_{i,j} x_{ij}$$

$$\sum_j x_{ij} = 1$$

$$\sum_j x_{ij}\, d_{ij} + wd_i < wd_k \quad \forall\, k \in fanout(i)$$

$$wd_k = U \quad \forall \quad k \in PO$$

$$x_{ij} \in \{0,1\}$$

where,

$d_{ij} = \mu + k\sigma$ number for gate i corresponding to level of correction j,

c_{ij} = cost of correction number for gate i corresponding to level of correction j,

$x_{ij} = 1$ if gate i is corrected to level j,

wd_i = worst case $\mu + k\sigma$ delay at input of gate i, calculated using STA, and

$U = \mu + k\sigma$ delay upper bound at the primary outputs (POs).

32. The medium as defined in claim 31 wherein said correction algorithm is based on an assumption that

$$\mu_{1+2} + k\sigma_{1+2} = \mu_1 + k\sigma_1 + \mu_2 + k\sigma_2$$

where $\mu+k\sigma$ is where μ is the mean, σ is the standard deviation of the performance distribution of gates, and $\mu+k\sigma$ denotes a certain level of parametric yield.

33. A machine readable medium for storing a program in a system for performing a mask design layout resolution enhancement in which a level of correction for the mask design layout for a predetermined parametric yield with a minimum total correction cost is determined, and the mask design layout is corrected at the determined level of correction based on the program on the medium if the level of correction is determined to be required, said program comprising:

mapping at least an area, a nominal delay, a cycle time and a die area of a gate sizing problem with a cost of correction, delay $\mu+k\sigma$, selling point delay and total cost of resolution enhancement technique (RET), respectively; and

creating a yield library from said mapping.

34. A system for minimizing a cost of correction of a mask design layout, comprising:

analyzing means for obtaining a first probability density function of a signal arrival time at an output of the circuit on the mask design layout; and

correction means for determining a first level of correction of the mask design layout based a correction algorithm if said first probability density function does not satisfy said predetermined parametric yield with a minimum total correction cost.

35. The system as defined in claim 34 wherein said analyzing means is a statistical static timing analysis (SSTA).

36. The system as defined in claim 34 wherein said correction algorithm is provided on a machine readable medium and includes a mathematical programming problem expressed as,

$$Minimize \sum_{i,j} x_{ij}$$

$$\sum_j x_{ij} = 1$$

$$\sum_j x_{ij}\, d_{ij} + wd_i < wd_k \quad \forall\, k \in fanout(i)$$

$$wd_k = U \;\forall\; k \in PO$$

$$x_{ij} \in \{0,1\}$$

where,

$d_{ij} = \mu + k\sigma$ number for gate i corresponding to level of correction j,

c_{ij} = cost of correction number for gate i corresponding to level of correction j,

$x_{ij} = 1$ if gate i is corrected to level j,

wd_i = worst case $\mu + k\sigma$ delay at input of gate i, calculated using STA, and

$U = \mu + k\sigma$ delay upper bound at the primary outputs (POs).

37. The system as defined in claim 36 wherein said correction algorithm is based on an assumption that

$$\mu_{1+2} + k\sigma_{1+2} = \mu_1 + k\sigma_1 + \mu_2 + k\sigma_2$$

where $\mu+k\sigma$ is where μ is the mean, σ is the standard deviation of the performance distribution of gates, and $\mu+k\sigma$ denotes a level of parametric yield.

38. The system as defined in claim 34 wherein said correction algorithm is provided on a machine readable medium and stores a program for,

mapping at least an area, a nominal delay, a cycle time and a die area of a gate sizing problem with a cost of correction, delay $\mu+k\sigma$, selling point delay and total cost of resolution enhancement technique (RET), respectively; and

creating a yield library from said mapping.